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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/152,266	09/14/1998	ERIC R. CAMPBELL	540-127	8971
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NIXON & VANDERHYE, PC 1100 N GLEBE ROAD 8TH FLOOR ARLINGTON, VA 22201-4714			EXAMINER PHAM, THOMAS K	
			ART UNIT 2121	PAPER NUMBER

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/152,266

Applicant(s)

CAMPBELL ET AL.

Examiner

Thomas K Pham

Art Unit

2121

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2-19 and 22-41 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2-16, 39 and 41 is/are allowed.
- 6) ☒ Claim(s) 17-19, 22-27, 29-38 and 40 is/are rejected.
- 7) ☒ Claim(s) 28 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

***Response to Amendment***

1. This action is in response to request for continued examination filed on 09/24/2004.
2. Claims 2-19 and 22-41 are presented for examination.

**Quotations of U.S. Code Title 35**

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

### **Claim Rejections - 35 USC § 102**

7. Claims 17-19, 22-27, 29-38 and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 5,469,549 ("Simpson").

#### **Regarding claims 17 and 22**

Simpson teaches an activity scheduler arranged to control activities in a processor, comprising:

- an integrated circuit to support shared data and multi-tasking for the processor (col. 3 lines 35-36, "The KEC supports ... into a single processor"), the integrated circuit comprising a set of stim-wait channels for each activity and arranged to support a control node mechanism (col. 3 lines 37-42, "It is also able to ... at each reschedule point"),
- each stim-wait channel responsive to a wait signal and a stim signal to control one of said activities (col. 5 lines 23-25, "A control\_node record type ... by another ACTIVITY"), and
- the integrated circuit further incorporating next activity logic to identify each activity that is ready to run on the processor (col. 13 lines 30-32, "Search logic identifies ... included activity number").

#### **Regarding claims 23 and 38**

Simpson teaches an activity scheduler arranged to control activities in a plurality of processors, comprising:

- a separate integrated circuit to support shared data and multi-tasking for each of said processors (col. 3 lines 35-36, "The KEC supports ... into a single processor"),

Art Unit: 2121

- each integrated circuit comprising a set of stim-wait channels for each activity and arrange to support a control node mechanism (col. 3 lines 37-42, “It is also able to ... at each reschedule point”),
- each stim-wait channel responsive to a wait signal and a stim signal to control one of said activities col. 5 lines 23-25, “A control\_node record type ... by another ACTIVITY”),  
and
- each of said separate integrated circuits further incorporating next activity logic to identify each activity that is ready to run on the associated processor (col. 13 lines 30-32, “Search logic identifies ... included activity number”).

**Regarding claim 24**

Simpson teaches an activity scheduler arranged directly to support shared data and multi-tasking in a network of processors, comprising:

- a separate integrated circuit to support each of said processors (col. 3 lines 35-36, “The KEC supports ... into a single processor”),
- each integrated circuit being configured to control a control node mechanism comprising a set of stim-wait channels (col. 3 lines 37-42, “It is also able to ... at each reschedule point”),
- each stim-wait channel incorporating holding means to hold a pair of control variables for one of said activities (col. 13 lines 35-38, “Each CEC holds ... stimulus to each side”),  
and

Art Unit: 2121

- each of said separate integrated circuits further incorporating next activity logic to identify each activity that is ready to run on the associated processor (col. 13 lines 30-32, "Search logic identifies ... included activity number").

**Regarding claim 25**

Simpson teaches at least one of said processors is arranged to set at least one control variable in one of said separate integrated circuits (col. 4 lines 15-18, "The KEC contains two ... a candidate for scheduling").

**Regarding claims 18, 26 and 40**

Simpson teaches a peripheral device arranged to set at least one control variable in one of said separate integrated circuits (col. 3 lines 29-30, "Synchronous Devices (peripherals which can generate an external stimulus) 45").

**Regarding claim 19**

Simpson teaches a multiprocessor network comprising a plurality of processors (fig. 2) each responsive to an activity scheduler, wherein the activity schedulers are linked together (col. 4 lines 1-5, "The KEC is able to ... 8 ACTIVITIES at each level").

**Regarding claim 27**

Simpson teaches at least one of said separate integrated circuits is arranged to set at least one control variable in another of said separate integrated circuits (col. 9 lines 16-22, "The mechanism for handling ... cause an ACTIVITY to run").

**Regarding claims 29 and 35**

Simpson teaches the control variables are Boolean (col. 4 lines 15-18, "The KEC contains two ... a candidate for scheduling").

Art Unit: 2121

**Regarding claim 30**

Simpson teaches including inhibitor means operable to inhibiting any changes to control variables from entering the next-activity-selection logic (col. 9 lines 53-66, “An exec ACTIVITY must be ... at the highest priority level”).

**Regarding claim 31**

Simpson teaches incorporating decoding and encoding logic to identify one or more of said activities and to route signals from said activity scheduler to the appropriate stim-wait channel (col. 7 lines 5-44, “a given CEC is ... particular communication protocol”).

**Regarding claim 32**

Simpson teaches including activity selection means operable to select the next activity on a round robin basis (col. 4 line 10, “a round robin search is used to select the next ACTIVITY”).

**Regarding claim 33**

Simpson teaches including priority selection means to allocate different priorities to groups of activities, and to select the next of activities within a group on a round robin basis within that group (col. 13 lines 28-32, “There are eight priority levels ... included activity number”).

**Regarding claim 34**

Simpson teaches a priority detector to detect an activity having a priority higher than the priority of an activity being processed on one of said processors, the priority detector being arranged to generate an interrupt signal to interrupt processing of the lower priority activity in favour of the higher priority activity (col. 4 lines 1-10, “The KEC is able to ... select the next ACTIVITY” ).

**Regarding claims 36 and 37**

Art Unit: 2121

Simpson teaches a method of controlling activities in a processor comprising holding a plurality of pairs of control variables in respect of each activity within a processor (col. 13 lines 33-38, "The CEC enables asynchronous ... external stimulus to each side"), identifying the next activity to be run on the processor (col. 13 lines 5-7, "The KEC contains an activity ... against a fixed rule set"), and selecting the pair of control variables associated with the said next activity within a processor (col. 4 lines 1-10, "The KEC is able to ... select the next ACTIVITY").

## **Second Rejection**

### **Claim Rejections - 35 USC § 102**

8. Claims 36 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Perotto et al "An 8-bit Multitask Micropower RISC Core" August 1994, IEEE Journal of Solid State Circuits, Vol. 29 No. 8 ("Perotto").

#### **Regarding claims 36 and 37**

Perotto teaches a method of controlling activities in a processor comprising holding a plurality of pairs of control variables in respect of each activity within a processor (page 988 column 1, "As shown in Fig. 6, the microprocessor can be ... chosen by the programmer" [the microprocessor holds 8-bit control variables in respect to the 4 tasks which inherently each 2-bit (a pair) controlling a task]), identifying the next activity to be run on the processor (page 988 column 2, "The hardware scheduler is able to ... the four PEi switches."), and selecting the pair of control variables associated with the said next activity within a processor (page 989 column 1, "The microprocessor contains a call ... in the corresponding program counter").



***Allowable Subject Matter***

9. Claims 2-16, 39 and 41 are allowed.
10. Claim 28 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner *Thomas Pham*; whose telephone number is (571) 272-3689, Monday - Thursday from 6:30 AM - 5:00 PM EST or contact Supervisor *Mr. Anthony Knight* at (571) 272-3687.


Any response to this office action should be mailed to: **Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450**. Responses may also be faxed to the **official fax number (703) 872- 9306**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Thomas Pham**  
*Patent Examiner*

TP

November 8, 2004

  
**Anthony Knight**  
**Supervisory Patent Examiner**  
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